12-16-05 10/644125 CJC

Docket No.: 08211/0200248-US0
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Letters Patent of:
Rajaram Subramoniam

Patent No.: 6,958,712

Issued: October 25, 2005

For: LOW GATE COUNT 3GPP
CHANNELIZATION CODE GENERATOR

REQUEST FOR CERTIFICATE OF CORRECTION
PURSUANT TO 37 CFR 1.322

Attention: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Upon reviewing the above-identified patent, Patentee noted several patent office errors which should be corrected.

In the Specification:

Column 2, Line 38 (Approx.) After "signal" delete "1", and insert -- I, --.

Column 4, Line 33 (Approx.) After "reaches" delete "SF-I" and insert -- SF-1 --.

Column 4, Line 40-48 (Approx.) Delete "Code logic circuit 404 is arranged to evaluate the number of valid bits in the code number according to the SF. The number of valid bits (N) is equal to $\log_2$ (SF). For example, an SF of 2 corresponds to one valid bit, an SF of 4 corresponds to two valid bits, and an SF of 8 corresponds to three valid bits. The most significant valid bit from the code number signal (code) is moved to the bit 7

position of the right justified code number signal (rjcode). All bits other than the N most significant bits are adjusted to zero." and insert the same in Col.4, Line 39 after "(code).".

Column 5, Line 6 (Approx.) Delete "SF-I" and insert -- SF-1 --.

Column 9, Line 63, In Claim 14, delete "fist" and insert -- first --.

The error was not in the application as filed by applicant; accordingly no fee is required.

Enclosed please find copies of pages 3, 6, & 7of the Specification and page 9 of the claims.

Transmitted herewith is a proposed Certificate of Correction effecting such amendment. Patentee respectfully solicits the granting of the requested Certificate of Correction.

Dated: December , 2005

Respectfully submitted,

By_____

Flynn Barrison
Registration No.: 53,970
DARBY & DARBY P.C.
P.O. Box 5257
New York, New York 10150-5257
(206) 262-8919
(212) 527-7701 (Fax)
Attorneys/Agents For Applicant

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.	:	6,958,712 B1
APPLICATION NO.	:	10/644,125
ISSUE DATE	:	October 25, 2005
INVENTOR(S)	:	Rajaram Subramoniam

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Specification:

Column 2, Line 38 (Approx.) After "signal" delete "1", and insert -- I, --.

Column 4, Line 33 (Approx.) After "reaches" delete "SF-I" and insert -- SF-1 --.

Column 4, Line 40-48 (Approx.) Delete "Code logic circuit 404 is arranged to evaluate the number of valid bits in the code number according to the SF. The number of valid bits (N) is equal to $\log_2$ (SF). For example, an SF of 2 corresponds to one valid bit, an SF of 4 corresponds to two valid bits, and an SF of 8 corresponds to three valid bits. The most significant valid bit from the code number signal (code) is moved to the bit 7 position of the right justified code number signal (rjcode). All bits other than the N most significant bits are adjusted to zero." and insert the same in Col.4, Line 39 after "(code).".

Column 5, Line 6 (Approx.) Delete "SF-I" and insert -- SF-1 --.

MAILING ADDRESS OF SENDER:
Flynn Barrison
DARBY & DARBY P.C.
P.O. Box 5257
New York, New York 10150-5257

Column 9, Line 63, In Claim 14, delete "fist" and insert -- first --.

MAILING ADDRESS OF SENDER:
Flynn Barrison
DARBY & DARBY P.C.
P.O. Box 5257
New York, New York 10150-5257

15. (Original) The method of Claim 12, wherein the binary count comprises a number of bits that is equal to a first number, the stored code number comprises a number of bits that is equal to the first number, and wherein logically calculating the channelization code comprises:

providing a first of a plurality of AND signals, wherein the first of the plurality of AND signals is provided such that the first of the plurality of AND signals corresponds to a logical level of one when a first condition is satisfied and the first of the plurality of bits corresponds to a logical level of zero when the first condition is not satisfied, and wherein the first condition is satisfied when a most significant bit of the binary count and the least significant bit of the stored code number both correspond to zero;

providing each subsequent AND signal of the plurality of AND signals, wherein each subsequent AND signal of the plurality of AND signals is provided such that the next of the plurality of AND signals corresponds to a logical level of one when a next condition is satisfied and the next of the plurality of bits corresponds to a logical level of zero when the next condition is not satisfied, and wherein the next condition is satisfied when a next most significant bit of the binary count and the next least significant bit of the stored code number both correspond to zero;

providing a first of a plurality of XOR signals, wherein the first of the plurality of XOR signals is provided such that the first of the plurality of XOR signals corresponds to a logical level of one when a first XOR condition is satisfied and the first of the plurality of bits corresponds to a logical level of zero when the first XOR condition is not satisfied, and wherein the first XOR condition is satisfied when the first of the plurality of AND signals corresponds to a logical level of one;

providing a next of the plurality of XOR signals, wherein the next of the plurality of XOR signals is provided such that the next of the plurality of XOR signals corresponds to a logical level of one when a next XOR condition is satisfied and the next of the plurality of bits corresponds to a logical level of zero when the next XOR condition is not satisfied, the next XOR condition is satisfied when the next of the plurality of AND signals and the previous XOR signal each correspond to different logical levels, and wherein the last of the plurality of XOR signals corresponds to the channelization code.

to the spreading factor minus one. A channelization logic circuit is configured to convert the binary count and the stored right-justified code number into the channelization code. According to one example, the channelization logic circuit comprises eight AND gates and eight XOR gates. A channelization code generator circuit may be integrated into an integrated chip that has a small silicon area and low power consumption.

FIG. 1 illustrates a circuit (100) for uplink modulation. Each of a plurality of data channels ($DPDCH_1$-$DPDCCH_6$) is multiplied by a channelization code ($C_{d,1}$ through $C_{d,6}$ respectively), and a gain (β_d) is applied to each of the channels. Each of the channelization codes ($C_{d,1}$ through $C_{d,6}$) is generated by a separate channelization code generator circuit (400). A control channel (DPCCH) is multiplied by a channelization code (Cc) and a gain (βc) is applied to the control channel. Channels $DPDCH_1$, $DPDCH_3$ and $DPDCH_5$ are summed to provide signal I, and channels $DPDCH_2$, $DPDCH_4$, $DPDCH_6$ and DPCCH are summed to provide signal Q. Signal Q is rotated by 90 degrees and summed with signal I to provide a combined signal. The combined signal is scrambled to provide a scrambled signal (S) by multiplying the combined signal by a scrambling code ($S_{dpch,n}$). The data is broadcast after the combined data from the data channels are scrambled.

Data that is broadcast via circuit 100 may be received by a mobile device via a circuit for downlink modulation (e.g. a rake receiver) (not shown). At least two channelization code generator circuits are required in the circuit for downlink modulation. One channelization code generator circuit is required for the data channel and one channelization code generator circuit is required for the control channel for a rake receiver with a single finger. Each additional data channel requires one additional channelization code generator circuit. To support 384Kbps, there are 3 data channels and one control channel for each finger. For optimal performance, the rake receiver has 6-8 fingers.

FIG. 2 illustrates the 3GPP definition of a channelization code in the form of a matrix. FIG. 3 illustrates the 3GPP definition of a channelization code in the form of a code tree.

coupled to node N33, and an output that is coupled to node N34. XOR gate X5 has a first input that is coupled to node N26, a second input that is coupled to node N34, and an output that is coupled to node N35. XOR gate X6 has a first input that is coupled to node N27, a second input that is coupled to node N35, and an output that is coupled to node N36. XOR gate X7 has a first input that is coupled to node N28, a second input that is coupled to node N36, and an output that is coupled to node N3.

Binary counter circuit 402 and code logic circuit 404 are each configured to receive a spreading factor signal at node N1. According to one example, the spreading factor signal is an eight-bit binary signal that corresponds to SF. Binary counter circuit 402 is further configured to receive a clock signal at node N37. Code logic circuit 404 is further configured to receive a code number signal (code) at node N2. XOR gate X0 is configured to receive a signal that corresponds to a logical level of zero at node N29.

Binary counter circuit 402 is illustrated as an eight-bit binary counter. The binary counter circuit (402) is arranged as a modulo SF binary counter. The binary counter circuit (402) counts from 0 to SF-1 in response to the clock signal. The binary counter circuit (402) rolls back to 0 the next clock after the count reaches SF-1. Binary counter circuit 402 is configured to provide the binary count as a binary count signal at the output of binary counter circuit 402.

Code logic circuit 404 is arranged to provide a right justified code number signal (rjcode) in response to the SF signal and the code number signal (code). Code logic circuit 404 is arranged to evaluate the number of valid bits in the code number according to the SF. The number of valid bits (N) is equal to $\log_2$ (SF). For example, an SF of 2 corresponds to one valid bit, an SF of 4 corresponds to two valid bits, and an SF of 8 corresponds to three valid bits. The most significant valid bit from the code number signal (code) is moved to the bit 7 position of the right justified code number signal (rjcode). All bits other than the N most significant bits are adjusted to zero.

For example, rjcode corresponds to 01100000 when the channelization code corresponds to $C_{ch,8,3}$. In this example, three bits are used since the SF is 8, the

code number corresponds to 011, and the most significant bit is adjusted to bit 7, so that bits 7, 6, and 5 corresponds to 0, 1, and 1 respectively. All bits other than the three most significant bits are adjusted to zero.

Register circuit 406 is arranged to store the right-justified code number. Register circuit 406 is configured to provide the stored right-justified code number as a stored code number signal at the output of register circuit 406.

Channelization logic circuit 408 is configured to provide the channelization code signal in response to the stored code number signal and the binary count signal. Channelization logic circuit 408 is configured to provide the channelization code signal in a serial manner. The first element of the channelization code is generated at a first clock pulse (i.e. when the binary count corresponds to zero). Each subsequent element of the channelization code is generated at each subsequent clock pulse (i.e. when the binary count increments). Channelization logic circuit 408 provides the first element of the channelization code again after all of the elements of the channelization code have been generated (i.e. when the binary count has reset to zero after reaching SF-1). A digital value of 0 corresponds to a channelization code element of "-1", while a digital value of 1 corresponds to a channelization code element of "1".

According to a further example, binary counter circuit 402 includes a digital comparator that is configured to compare the binary count to SF-1. According to this example, an output of the digital comparator is coupled to a reset input of the binary counter such that the binary counter is reset to 0 when the binary count corresponds to SF-1.

According to one example, binary counter circuit 402 is configured to receive a frame reset signal. The binary counter is reset to 0 when either the frame reset signal corresponds to an active level or the signal provided by the digital comparator output corresponds to an active level. For example, binary counter circuit 402 may further include an OR gate having a first input, a second input, and an output. The first input is configured to receive the frame reset signal, the second input is coupled to the

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